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EXAMINER	
YANG, LINA	
ART UNIT	**PAPER NUMBER**
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,160	YAVATKAR ET AL.	
	Examiner	Art Unit	
	Lina Yang	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/24/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3-5, 8, 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Alley et al (U. S. Patent No. 6,487,264 B1).

Regarding claim 1, Alley teaches a system to manage energy usage of processor (fig. 1 and the energy is managed through the control means 24 in fig. 2; col. 6 lines 39-50 and col. 7 lines 21-25), comprising:

a data communication network (fig.1; col. 2 lines 35-57);

a transmitter (RF modem A or B or C... or n in fig. 1 and fig. 11, the modem is both a transmitter and receiver controlled by decoupling means 34 in fig. 3), coupled to the data communication network (fig. 1), to invoke a protocol state machine (the transmitter logic contains the Manchester Encoder 120 in fig. 11) to send a packet, to wait for an acknowledgment of receipt (fig. 19), and to prepare for a periodic transmission of additional packets (fig. 19 and the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28);

a receiver (RF modem A or B or C... or n in fig. 1 and fig. 12, the modem is both a transmitter and receiver controlled by decoupling means 34 in fig. 3), in communication with the transmitter coupled to the data communication network (fig. 1), to receive, process, and verify the packet and send an acknowledgment of receipt (fig. 19 and the corresponding explanation in col. 11, 12);

a buffer, coupled to the (the Manchester Encoder 120 in fig. 11), to store the packet (fig. 11 element 114); and

a timer (clock logical 106 in fig. 9 and fig. 10), in communication with the transmitter and the receiver, to cause a periodic pattern of packet transmission and reception, wherein the processor is adapted for use in an energy conscious device (col. 7 lines 21-62) .

Regarding claim 3, Alley further teaches that the transmitter begins in a high power, high clock rate mode (fig. 19 start from time 3).

Regarding claim 4, Alley further teaches that the transmitter performs tasks to create packets for transmission (fig. 11; col. 8 lines 21-67 and col. 12 lines 50-55).

Regarding claim 5, Alley further teaches that the tasks include at least one of dividing data into packets (col. 12 lines 50-55), adding protocol headers (headers in fig. 20 and 21; col. 12 lines 3-21 and 41-62), and computing checksums (CRC in fig. 20 and 21).

Regarding claim 8, Alley further teaches that the receiver begins in a low power, low clock rate mode (fig. 19, starting time 1).

Regarding claim 10, Alley further teaches that a frequency setting and a power level of the processor are determined by the transmitted or received packet (fig. 19).

Regarding claim 11, Alley further teaches that the periodic pattern in packet transmission and reception are used to manage the frequency setting and power level of the processor (fig. 19 the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 12-13, 16-19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Khanna (U. S. Patent No. 5,978,849).

Regarding claims 2 and 22, Alley does not specifically teach that the data communication network includes at least one of the Internet and an Intranet. However, Alley teaches that the information is to be transferred from one location to another, such as computer-to-computer (col. 1 lines 12-16). And it's well known in the art that when the information is to be transferred from one location to another, then the data communication network either includes Internet (when public networks are involved), intranet (when only private networks are involved) or both. For example, Khanna teaches that computer-to-computer communication involves Internet and/or Intranets (fig. 1 and col. 3 lines 59-62). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to specify that the data communication network includes at least one of the Internet and an Intranet, as taught

by Khanna in the assembly of Alley in order to cover the most common communication environments.

Regarding claim 12, Alley teaches

sending a data packet over a data communication network to a receiver protocol state machine (the receiver logic that contains Manchester Decoder 126 in fig. 12) that stores the data packet in an application buffer (129 in fig. 12) (fig. 1; fig. 11; fig. 12 and fig. 19);

waiting for an acknowledgment of receipt of the data packet from the receiver protocol state machine (the receiver logic that contains Manchester Decoder 126 in fig. 12) (fig. 19 and the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28); and

arranging for a transmission of additional data packets (fig. 19 and the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28).

Alley does not teach that a storage medium having stored thereon instructions that when-executed by a machine result in the above limitations. However, it is with the level of one skilled in the art to implement the logic as software or computer program instructions. It would have been obvious to one of ordinary skill at the time of the invention to store the computer program instructions on a computer readable media so they are executable on a processor.

Regarding claim 13, Alley further teaches that the transmitter begins in a high power, high clock rate mode (fig. 19 start from time 3).

Regarding claims 16 and 21, Alley further teaches that an application buffer (114 in fig. 11) and a timer (fig. 10) cause periodic patterns in data packet transmission, which are used to manage power and frequency of a processor (fig. 19 and the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28).

Regarding claim 17, Alley teaches

receiving a data packet from a transmitter protocol state machine (the transmitter logic that contains Manchester Encoder 120 in fig. 11) over a data communication network (fig. 1; fig. 12 and fig. 19);

depositing the data packet in an application buffer (129 in fig. 12; col.9 lines 41-56);

processing and verify the data packet (col.9 lines 41-56);

and

transmitting an acknowledgment of receipt of the data packet to the transmitter protocol state machine (the transmitter logic that contains Manchester Encoder 120 in

fig. 11), wherein the transmitter protocol state machine prepares for transmission of additional data packets (fig. 19; and the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28).

Alley does not teach that a storage medium having stored thereon instructions that when-executed by a machine result in the above limitations. However, it is with the level of one skilled in the art to implement the logic as software or computer program instructions. It would have been obvious to one of ordinary skill at the time of the invention to store the computer program instructions on a computer readable media so they are executable on a processor.

Regarding claim 18, Alley further teaches all the limitations (referring to the rejection of claim 17) except that the instructions are provided to a receiver protocol state machine to obtain delivery of the data packet, to store the data packet in the application buffer, to process the data packet, and to send the acknowledgment of receipt of the data packet. However, it is with the level of one skilled in the art to implement the logic as software or computer program instructions. It would have been obvious to one of ordinary skill at the time of the invention to store the computer program instructions on a computer readable media so they are executable on a processor.

Regarding claim 19, Alley further teaches that the receiver protocol state machine (the receiver logic that contains Manchester Decoder 126 in fig. 12) to enter an idle low power, low clock rate mode upon obtaining delivery of the data packet (fig. 19, receiver B returns to idle after time 19).

3. Claims 6-7, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Mantha et al (U. S. Patent Application Publication No. 20030126551)

Regarding claims 6 and 14, Alley does not specifically teach that the transmitter enters a low power, low clock rate mode while waiting for an acknowledgment from the receiver. However, Mantha teaches that the transmitter sends out a frame (packet) and waits in a idle state waiting for an ACK ([0110]). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the transmitter enters a low power, low clock rate mode while waiting for an acknowledgment from the receiver, as taught by Mantha in the assembly of Alley in order to save the memory in either the transmitter or the receiver.

Regarding claims 7 and 15, Alley further teaches that the transmitter awakens as at least one of a timer sounds and an incoming packet buffer reaches a low water mark (timer 108 activating the wakeup logic 110 after a programmed number of slow clock pulses; col. 7 lines 34-49).

4. Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Marko et al (U. S. Patent No. 6,876,835 B1)

Regarding claims 9 and 20, Alley does not specifically teach that the receiver enters a high power, high clock rate mode when the buffer reaches capacity or a high water mark. However, Alley teaches that the receiver enters a high power, high clock rate mode after a predetermined time (see fig. 190) and suggested that other programmed scenarios can be used. For example, Marko teaches that a receiver can be programmed with a wake-up feature when the local storage buffer reaches a certain threshold (col. 8 lines 31-40). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the receiver enters a high power, high clock rate mode when the buffer reaches capacity or a high water mark, as taught by Marco in the assembly of Alley in order to automatically wake up to receive a message.

5. Claims 23-24 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Minami et al (U. S. Patent No. 6,034,963 B1)

Regarding claim 23, Alley teaches a method of managing energy usage of a processor using a transmitter protocol state machine and a receiver protocol state machine comprising

receiving the data packet (fig. 19 from time 2 to time 3, the modem receives the data packet from the attached host);

storing the data packet in at least one application buffer(element 120 in fig. 11);

switching a processor clock mode and a power mode (to active mode starting time 3 in fig. 19);

processing the buffered data packet ((fig. 11; col. 8 lines 21-67 and col. 12 lines 50-55);

transmitting the processed data packet (fig. 19 time 160 and time 170); and

delivering the processed data packet to the data communication network (fig. 19 time 160 and time 170).

Alley does not specifically teach that a plurality of transmitter protocol state machines and a plurality of receiver protocol state machines in a multiple layer architecture within a data communication network are used, and the relaying, from the plurality of transmitter protocol state machines, a data packet to a receiver protocol state machine. However, Minami teaches that multiple transmitter protocol state machines and a plurality of receiver protocol state machines will be used to simultaneously encode (decode) the packets with multiple applications with same or

multiple protocols are transmitted and received in a network (fig. 1, col. 3 lines 46- 51). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to use a plurality of transmitter protocol state machines and a plurality of receiver protocol state machines in a multiple layer architecture within a data communication network, as taught by Minami in the assembly of Alley in order to process the packets simultaneously to achieve high performance.

Regarding claim 24, the modified assembly of Alley and Minami further teaches that the plurality of transmitter protocol state machines commence at an appropriate clock rate for one application among a plurality of applications (by default, each application has an appropriate clock rate).

Regarding claim 29, the modified assembly of Alley and Minami further teaches that the plurality of transmitter protocol state machines begin in a high power, high clock rate mode (Alley: fig. 19 start from time 3), and the plurality of receiver protocol state machines begin a low power, low clock rate mode (Alley: fig. 19 start from time 1)..

Regarding claim 30, the modified assembly of Alley and Minami further teaches that the data communication network is at least one of the Internet and an Intranet (Forin: col. 9 lines 24-26).

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Minami et al (U. S. Patent No. 6,034,963 B1), as applied to claims 23 and 24, and further in view of Forin (U. S. Patent No. 6,594,701 B1).

Regarding claim 25, the modified assembly of Alley and Minami does not specifically teach that each application fills one application buffer in a plurality of application buffers. However, Forin teaches that each application fills one application buffer in a plurality of application buffers (a plurality of application-level buffers in fig. 2). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include each application fills one application buffer in a plurality of application buffers, as taught by Forin in the assembly of Alley and Minami in order to provide better buffer managements.

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Minami et al (U. S. Patent No. 6,034,963 B1) and Forin (U. S. Patent No. 6,594,701 B1), as applied to claims 23-25, and further in view of Todd (U. S. Patent No. 6,714,516 B1).

Regarding claim 26, the modified assembly of Alley, Minami and Forin does not specifically teach that the plurality of applications are blocked when at least one application buffer reaches capacity and all buffers contain sufficient data. However, it's

well known in the art that when a threshold of a receiver's buff is reached, the receiver will cease all the receiving. For example, Todd teaches that when the number of available buffers reaches certain predetermined threshold values, the receiver sends an indication to the transmitter to restrict its message transmit, thereby throttling the message flow therefrom (abstract). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include blocking the plurality of applications when at least one application buffer reaches capacity and all buffers contain sufficient data, as taught by Todd in the modified assembly of Alley, Minami and Forin in order to control the congestion.

8. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alley et al (U. S. Patent No. 6,487,264 B1) in view of Minami et al (U. S. Patent No. 6,034,963 B1), Forin (U. S. Patent No. 6,594,701 B1), and Todd (U. S. Patent No. 6,714,516 B1), as applied to claims 23-26, and further in view of Marko et al (U. S. Patent No. 6,876,835 B1).

Regarding claim 27, the modified assembly of Alley, Minami, Forin and Todd does not specifically teach that the plurality of receiver protocol state machines are invoked to process the data in the buffers. However, Marko teaches that a receiver can be programmed with a wake-up feature when the local storage buffer reaches a certain threshold (col. 8 lines 31-40). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include invoking the plurality

of receiver protocol state machines, as taught by Marco in the modified assembly of Alley, Minami, Forin and Todd in order to automatically wake up to receive a message.

Regarding claim 28. The method of claim 27, wherein the plurality of transmitter protocol state machines switch the processor clock mode and the power mode to an appropriate mode to process data (fig. 19 and the corresponding explanation in col. 11, 12 and 13 and col. 8 lines 23-28).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lina Yang whose telephone number is (571) 272-3151. The examiner can normally be reached Monday through Wednesday between 7:00 a.m. and 8:00 p.m. eastern standard time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LY

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